DESCRIPTION

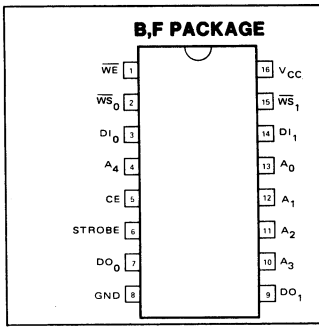
The 82S21 is a TTL 64-bit Write-While-Read Random Access Memory organized as 32 words of 2 bits each. The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5-input decoder when the CHIP enable input CE is at logic "1". $\overline{WS_0}$ and $\overline{WS_1}$ are the write select inputs for bit 0 and bit 1 of the word selected. TOE is the write enable input. When $\overline{WS_N}$ and $\overline{WE}$ are both at logic "0" data on the DI_0 and DI_1 data lines are written into the addressed word. The read function is enabled when either $\overline{WS_n}$ or $\overline{WE}$ is at logic "1".

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, Strobe, is logic "1" and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When Strobe goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When Strobe goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

PIN CONFIGURATION

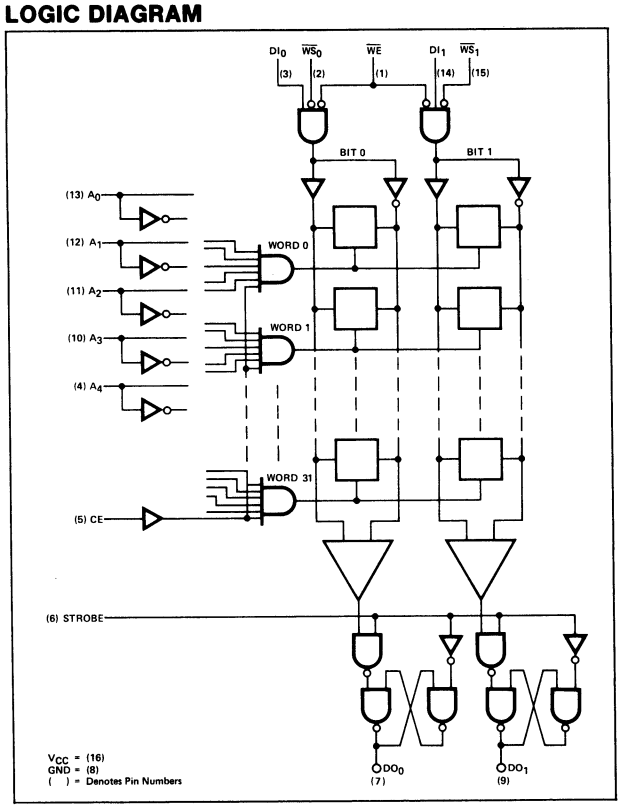
B,F PACKAGE



TRUTH TABLE

CE	$\overline{WE}$	$\overline{WS_0}$	$\overline{WS_1}$	STROBE	MODE	OUTPUTS
X	X	X	X	0	Output Hold	Data from last addressed word when CE = "1"
0	X	X	X	0	Disabled	Logic "1"
1	1	X	X	1 or ↓	Read (transparent/latched)	Data stored in addressed word
1	0	1	1	1 or ↓	Read (transparent/latched)	Data stored in addressed word
1	0	0	0	0	Write Data	Data from last word address when Strobe went from "1" to "0"
1	0	0	0	1	Write Data	Data being written into memory
1	0	0	1	X	Write Data into Bit 0 Only	If Strobe = 0: Data from last word address when Strobe went from "1" to "0"
1	0	1	0	X	Write Data into Bit 1 Only	If Strobe = 1: Data being written into the selected bit, or stored in the addressed location.

LOGIC DIAGRAM



AC ELECTRICAL CHARACTERISTICS $0 \leq T_A \leq$ $\leq V_{CC} \leq$

PARAMETER		LIMITS MIN	TYP	MAX
Read Access Time Address to Output	t_1		25	50
Address Set-Up Time	t_2		8	15
Data Set-Up Time	t_3		15	20
Address Hold Time	t_4			0
Control or Write Pulse Width	t_5		15	20
Write Access Time	t_6		20	25
Address to Latch Set-Up Time	t_7		25	50
Latch Address to Address Hold Time	t_8		7	10
Delatch Access Time	t_9		15	25
Data Hold Time	t_{10}		0	5