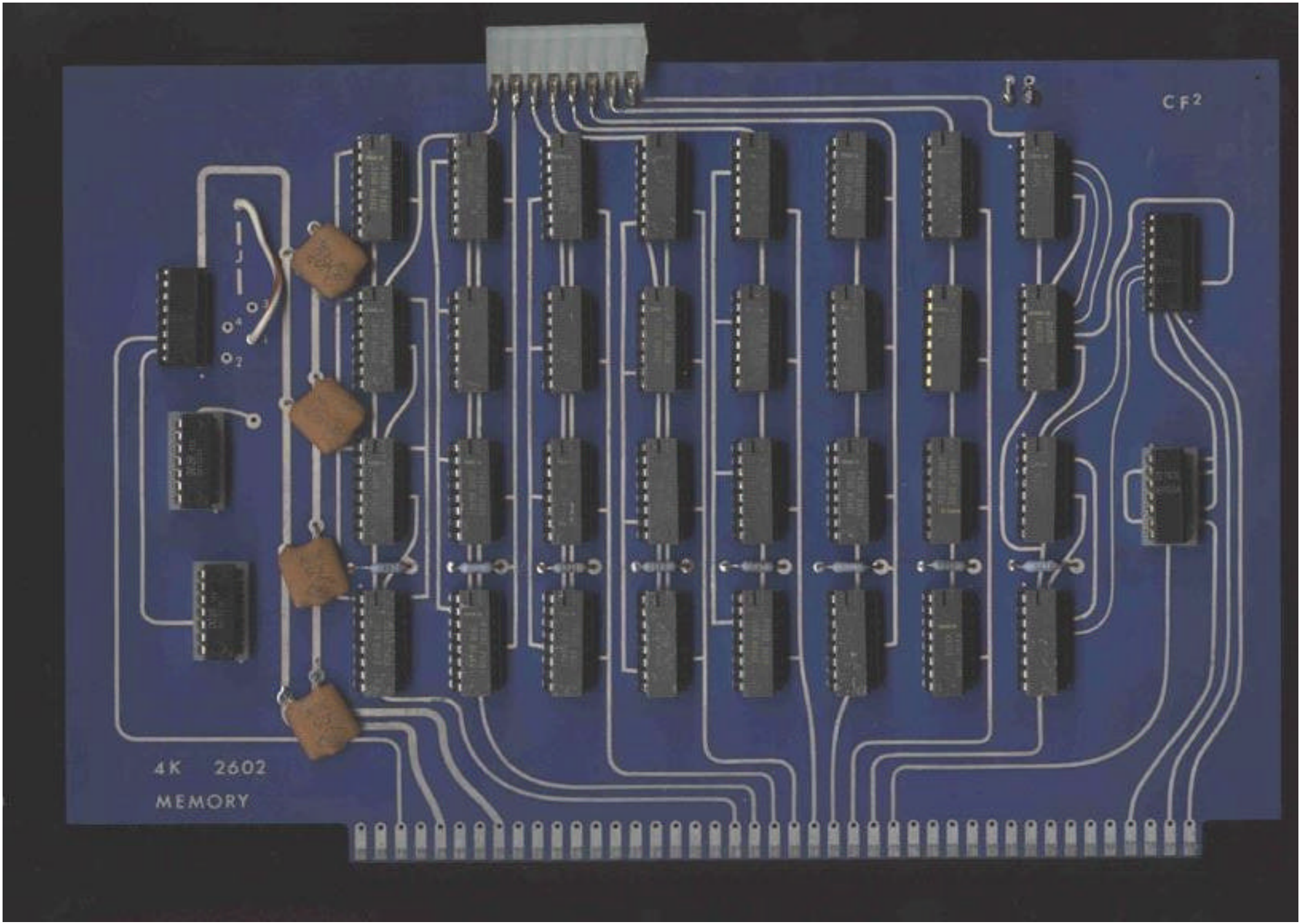
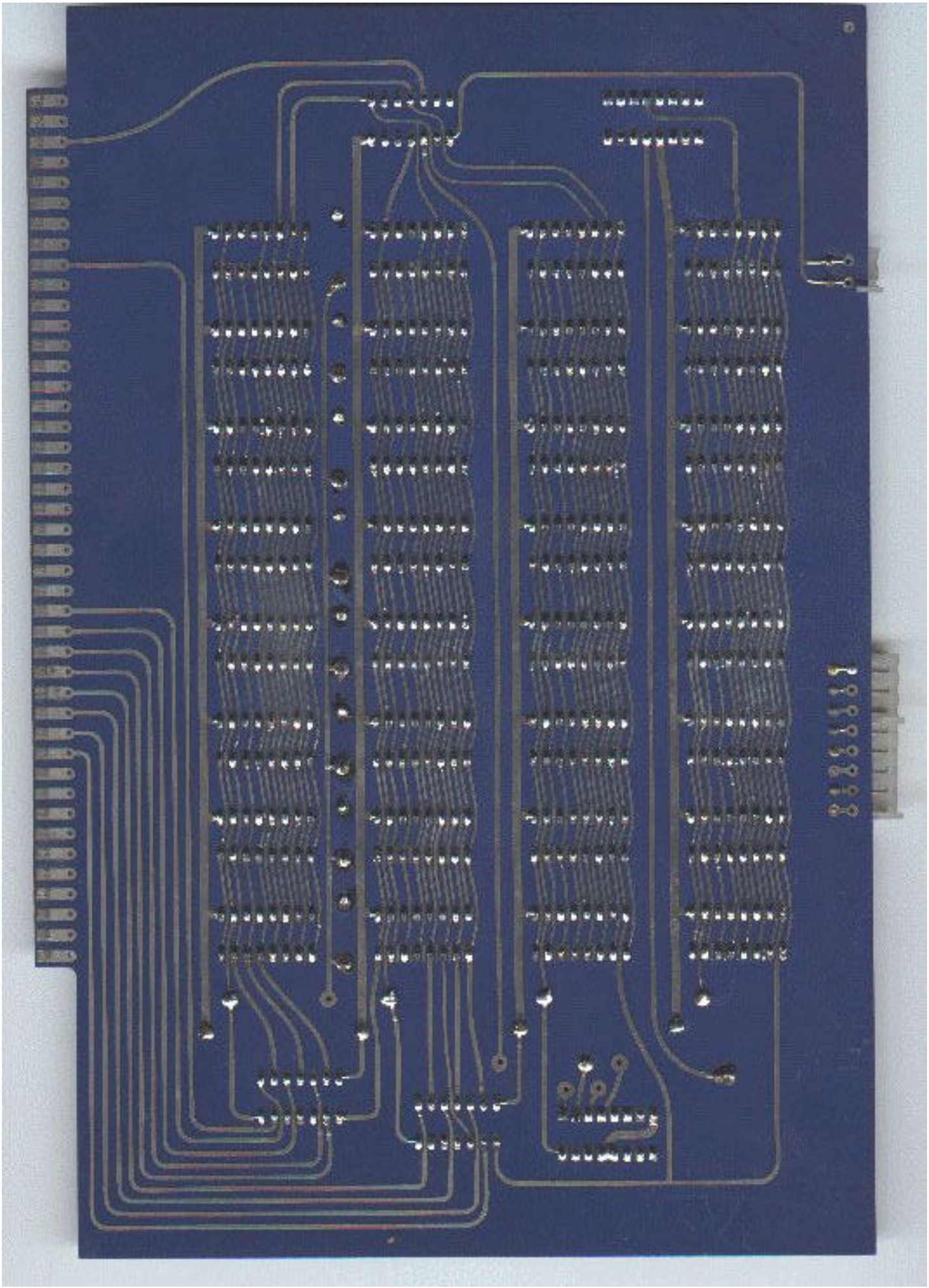
4K Memory for Mark-8 Minicomputer

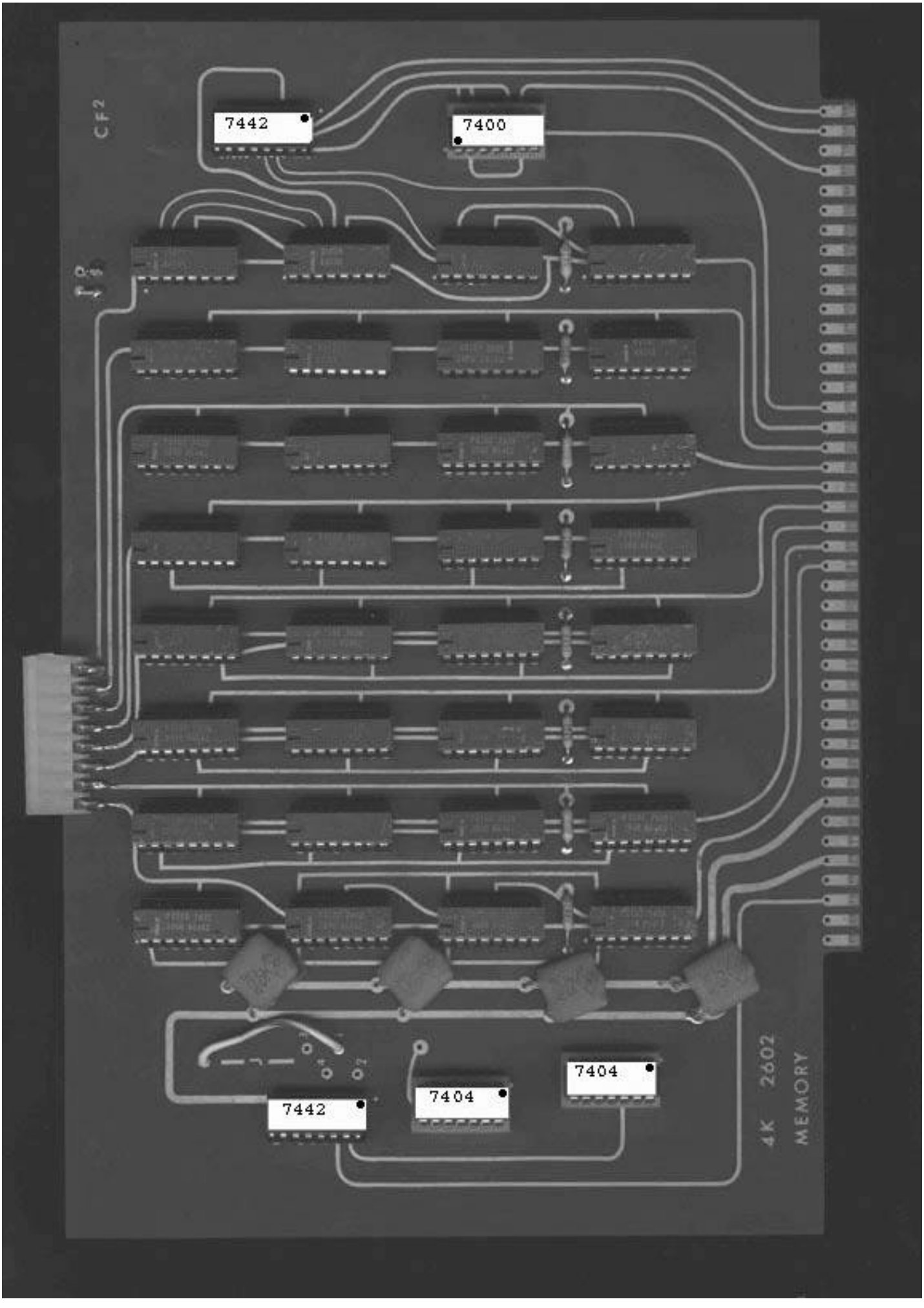
By Bryan Blackburn http://members.cox.net/oldcomp/

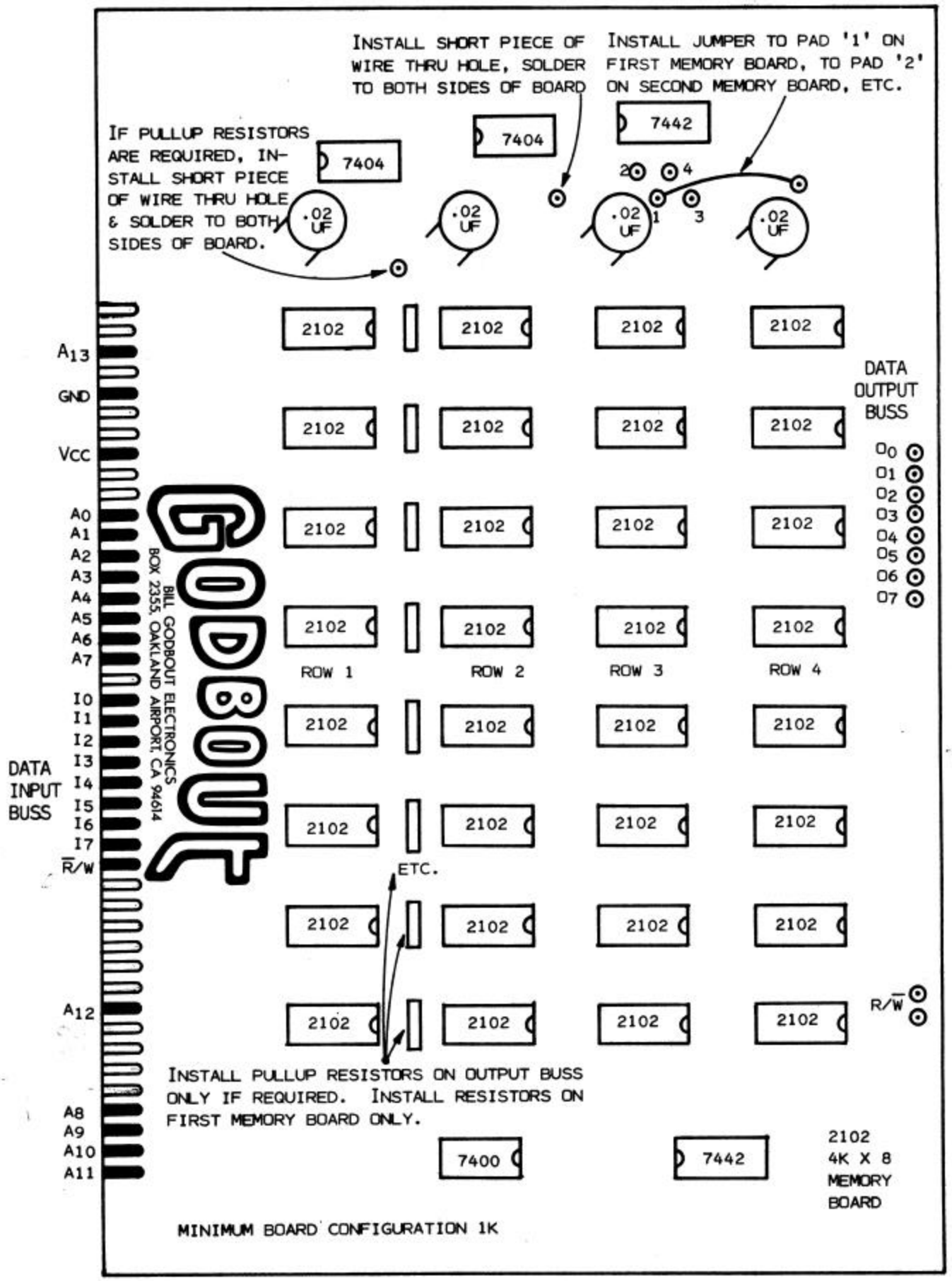
When I received my Mark-8 in little pieces from an eBay auction, I did not receive the original memory card. I received this one. It appears to have been made by Godbout Electronics, but confirmation is yet to come. It is certainly the same design, but is lacking the Godbout logo. Did Godbout buy this design from someone else? Did someone copy their design? If you would like to build one, there is enough information here to do so. I have included a few chip data sheets, they cmos versions, but the pinouts are the same. Good luck!

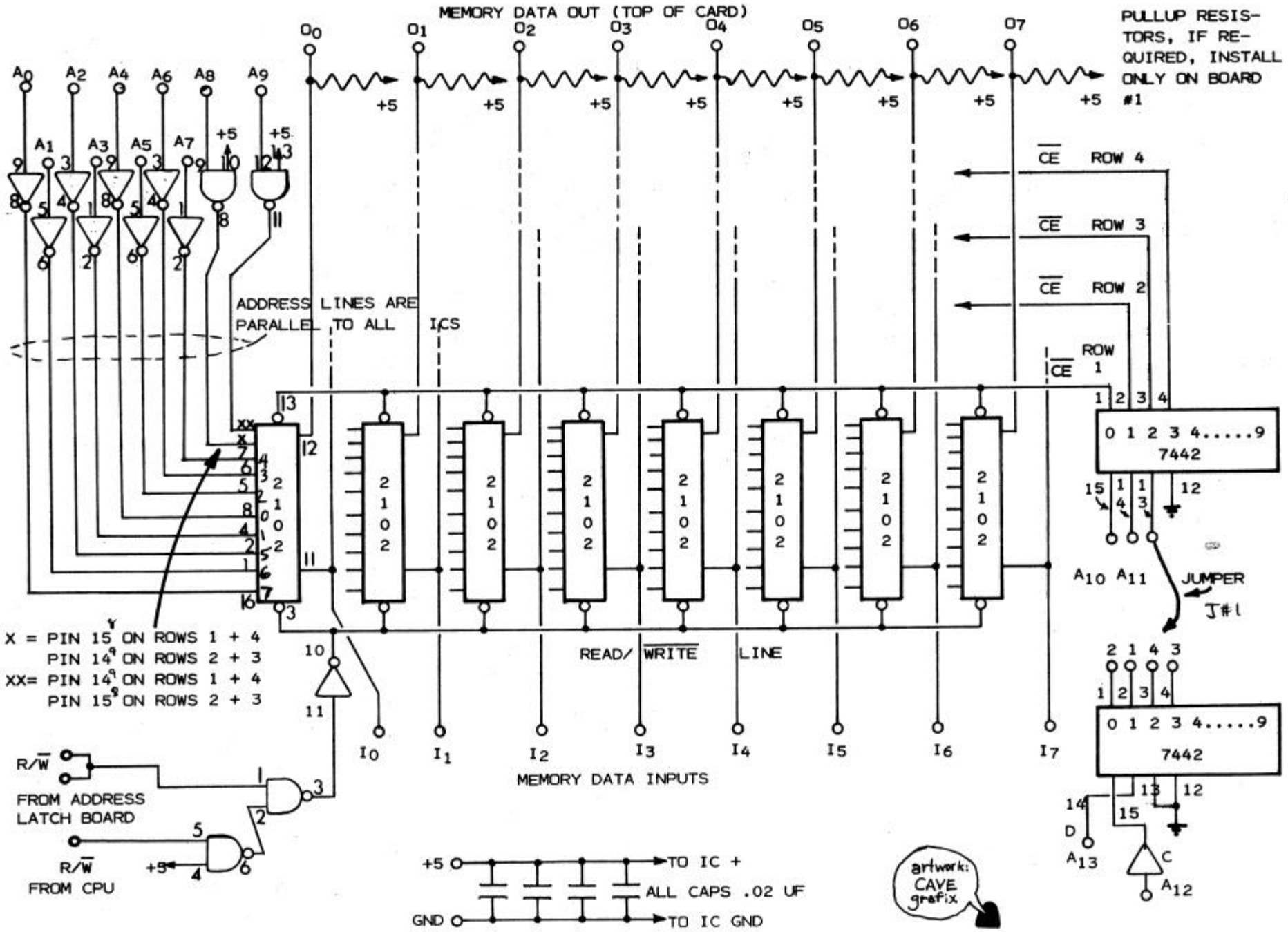
-Bryan


CF2
4K 2602
MEMORY




CF2
7442
7400
7442
7404
7404
4K 2602
MEMORY


INSTALL SHORT PIECE OF WIRE THRU HOLE, SOLDER TO BOTH SIDES OF BOARD
INSTALL JUMPER TO PAD '1' ON FIRST MEMORY BOARD, TO PAD '2' ON SECOND MEMORY BOARD, ETC.
IF PULLUP RESISTORS ARE REQUIRED, INSTALL SHORT PIECE OF WIRE THRU HOLE & SOLDER TO BOTH SIDES OF BOARD.
7404
7404
7442
.02 UF
.02 UF
.02 UF
.02 UF
2
4
1
3
2102
ROW 1
ROW 2
ROW 3
ROW 4
ETC.
DATA OUTPUT BUSS
O0
O1
O2
O3
O4
O5
O6
O7
R/W
DATA INPUT BUSS
A13
GND
Vcc
A0
A1
A2
A3
A4
A5
A6
A7
I0
I1
I2
I3
I4
I5
I6
I7
R/W
A12
A8
A9
A10
A11
GODBOUT
BILL GODBOUT ELECTRONICS
BOX 2355, OAKLAND AIRPORT, CA 94614
INSTALL PULLUP RESISTORS ON OUTPUT BUSS ONLY IF REQUIRED. INSTALL RESISTORS ON FIRST MEMORY BOARD ONLY.
7400
7442
2102
4K X 8
MEMORY
BOARD
MINIMUM BOARD CONFIGURATION 1K


MEMORY DATA OUT (TOP OF CARD)
O0 O1 O2 O3 O4 O5 O6 O7
PULLUP RESISTORS, IF REQUIRED, INSTALL ONLY ON BOARD #1
+5
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
ADDRESS LINES ARE PARALLEL TO ALL ICS
CE ROW 4
CE ROW 3
CE ROW 2
CE ROW 1
2102
0 1 2 3 4.....9
7442
A10 A11
JUMPER J#1
X = PIN 15 ON ROWS 1 + 4
PIN 14 ON ROWS 2 + 3
XX= PIN 14 ON ROWS 1 + 4
PIN 15 ON ROWS 2 + 3
READ/ WRITE LINE
I0 I1 I2 I3 I4 I5 I6 I7
MEMORY DATA INPUTS
R/W
FROM ADDRESS LATCH BOARD
R/W
FROM CPU
+5
TO IC +
ALL CAPS .02 UF
GND
TO IC GND
D
A13
C
A12
artwork: CAVE grafix

National Semiconductor

MM54C42/MM74C42 BCD-to-Decimal Decoder

General Description

The MM54C42/MM74C42 one-of-ten decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. This decoder produces a logical "0" at the output corresponding to a four bit binary input from zero to nine, and a logical "1" at the other outputs. For binary inputs from ten to fifteen all outputs are logical "1".

- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 50 nW (typ.)
- Medium speed operation — 10 MHz (typ.) with 10V V_{CC}

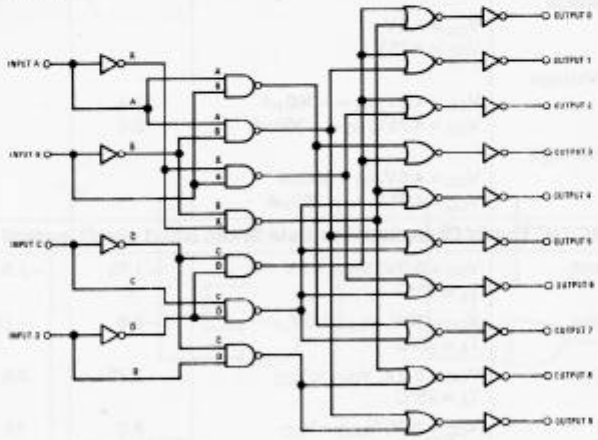
Features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads

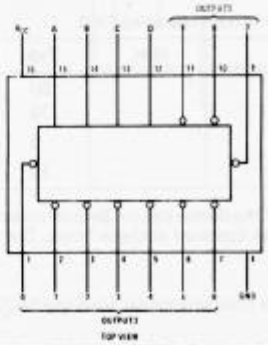
Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Schematic Diagram



Connection Diagram



Truth Table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	H	L	H	H	H	H	H	H	H	H
L	L	L	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	H	H	H	L	H	H	H	H	H	H
L	L	H	H	H	H	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	H	H	H	H	H	H	L	H	H	H
L	H	H	L	H	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	H	H	H	L	H
H	L	L	L	H	H	H	H	H	H	H	H	H	L
H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

National Semiconductor

MM54C00/MM74C00 Quad 2-Input NAND Gate
MM54C02/MM74C02 Quad 2-Input NOR Gate
MM54C04/MM74C04 Hex Inverter
MM54C10/MM74C10 Triple 3-Input NAND Gate
MM54C20/MM74C20 Dual 4-Input NAND Gate

General Description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

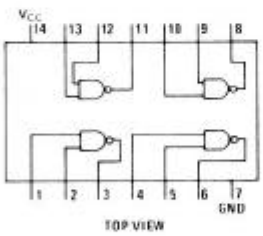
Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power consumption	10nW/package (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

1

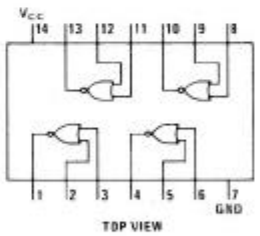
Connection Diagrams

MM54C00/MM74C00



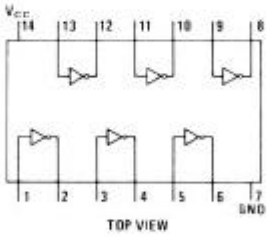
TOP VIEW

MM54C02/MM74C02



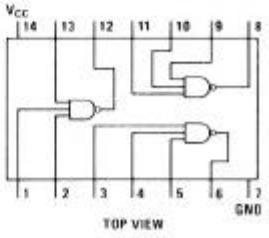
TOP VIEW

MM54C04/MM74C04



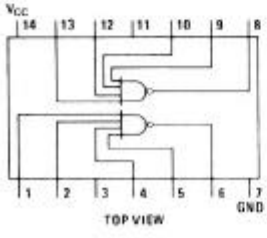
TOP VIEW

MM54C10/MM74C10



TOP VIEW

MM54C20/MM74C20



TOP VIEW

2102A, 2102AL/8102A-4*
1K x 1 BIT STATIC RAM

P/N	Standby Pwr. (mW)	Operating Pwr. (mW)	Access (ns)
2102AL-4	35	174	450
2102AL	35	174	350
2102AL-2	42	342	250
2102A-2	— —	342	250
2102A	— —	289	350
2102A-4	— —	289	450

- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Standby Power Mode (2102AL)**
- **Three-State Output: OR-Tie Capability**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Dual-In-Line Configuration**

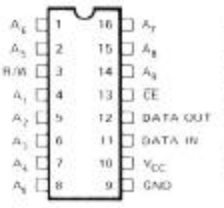
The Intel® 2102A is a high speed 1024 word by one bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. *A low standby power version (2102AL) is also available. It has all the same operating characteristics of the 2102A with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.*

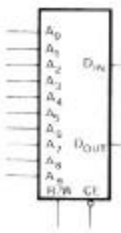
It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



LOGIC SYMBOL



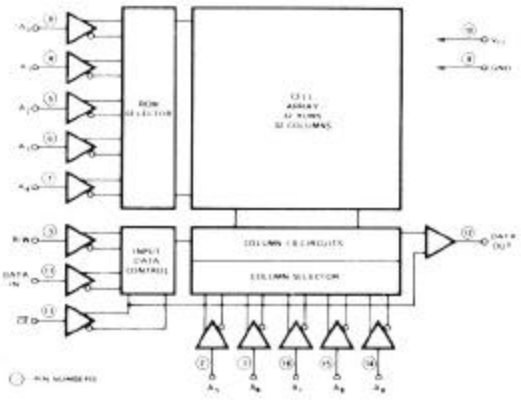
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

BLOCK DIAGRAM



*All 8102A-4 specifications are identical to the 2102A-4 specifications.